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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,745	07/21/2000	KARL AMUNDSON	INK-086-(2108/66)	4716

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EXAMINER	
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ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 06/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/621,745	AMUNDSON ET AL.	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 07/26/2001 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed limitations, "an encapsulated display medium comprising a plurality of pixels", "a transistor having a data electrode, a gate electrode and a pixel electrode and comprising a layer of insulating material situated between a first layer of conductive material that forms the gate electrode and a second layer of conductive material that forms the data and pixel electrodes" and "a storage capacitor comprising a layer of insulating material situated between a first layer of conductive material and a second layer of conductive material", as recited in claim 1, "wherein one of said layers of material comprising said transistor and a respectively layer of material comprising said storage capacitor comprise a continuous layer of material", as recited in claim 5, "a plurality of constinuous layers of material", as recited in claims 6 and 17, "wherein the storage capacitor comprises a storage capacitor pixel electrode, an insulator disposed adjacent the pixel electrode and a storage capacitor gate electrode disposed adjacent the insulator", as recited in claim 9, "the insulator is patterned", as recited in claim 10, "the insulator is unpatterned", as recited in claim

11, "wherein the storage capacitor comprises a storage capacitor pixel electrode, a semiconductor layer disposed adjacent the storage capacitor pixel electrode, an insulator disposed adjacent the semiconductor and a storage capacitor gate electrode disposed adjacent the insulator", as recited in claim 13, "wherein the storage capacitor comprises a storage capacitor pixel electrode, an insulator disposed adjacent the storage capacitor pixel electrode and a conductor disposed adjacent the insulator", as recited in claim 14, "an encapsulated electrophoretic display medium comprising a plurality of pixels", as recited in claim 18, "a display medium comprising a plurality of pixels", "applying an electric pulse ... pulse ends", as recited in claim 19, "wherein a plurality of electric pulses ... pulses end", as recited in claim 20, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. As noting in figures 4A-4B and at page 10, lines 11-23, the application discloses an exemplary embodiment of a transistor and a storage capacitor together. However, the drawing and the specification do not clearly specify which elements included in the transistor or in the storage capacitor, e.g., in figure 4B, a dashed box representing a transistor and showing all the elements of the transistor and the similar for the storage capacitor.

Claim Objections

4. Claim 1 is objected to because of the following informalities: line 7, "the transistor pixel electrode" should be changed to -- the pixel electrode -- so as to be consistent with the claimed limitation line 3. Appropriate correction is required.

5. Claim 20 is objected to because of the following informalities: line 2, "each pulse" should be changed to -- each of said plurality of electric pulses --, and line 4, "an electric pulse" should be changed to -- one of said plurality of electric pulses --, so as to be clarify each pulse or an electric pulse being one of the plurality of electric pulses recited in line 1 of claim 20. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per independent claim 1, it is not clear that a layer of insulating material in line 4 is the same as a layer of insulating material in line 8, a first layer of conductive material in lines 4-5 is the same as a first layer of conductive material in lines 8-9, a second layer of conductive material in line 5 is the same as a second layer of conductive material in line 9. It is suggested that if they are the same, --said-- should be used instead of "a", or if they are different, different names should be used.

As per claims 2-17, since these claims depend directly or indirectly on claim 1, these claims are also rejected for the same reason as set forth in claim 1 above.

In addition to claim 3, when this claim is read together with independent claim 1, this claim recites (1) a transistor and a storage capacitor each comprising three layers (see claim 1) and (2) one of said layers comprising said transistor and a layer comprising said storage

capacitor, i.e., the transistor comprising layers of material or a layer of material comprising the transistor, and the storage capacitor comprising layers of material or a layer of material comprising the storage capacitor.

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 6, 9-14, 17, 19 and 20 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claims 6 and 17, when these claims are respectively read together with independent claim 1, these claims recite comprising a layer of insulating material, a first layer of conductive material, a second layer of conductive material and at least one continuous layer of material, and a storage capacitor comprising a layer of insulating material, a first layer of conductive material, a second layer of conductive material and at least one continuous layer of material. The application discloses several embodiments, especially only the embodiment illustrated in figures 4A and 4B showing both structures of the transistor and the storage capacitor together. However, as noting in figures 4A and 4B and at page 10, the application does not describe the claimed limitations in such a way as to enable examiner to understand the claimed invention, e.g., which reference numbers in figures 4A-4B corresponding to the claimed insulating material layer of the claimed transistor, the claimed first conductive material layer of the claimed transistor, the claimed conductive materia second layer of the claimed transistor and

the claimed continuous material layer of the claimed transistor, and which reference numbers corresponding to the claimed insulating material layer of the claimed storage capacitor, the claimed first conductive material layer of the claimed storage capacitor, the claimed conductive material second layer of the claimed storage capacitor and the claimed continuous material layer of the claimed storage capacitor, as recited in the claims above.

As per claim 9, when this claim is read together with independent claim 1, this claim recites a storage capacitor comprising a layer of insulating material, a first layer of conductive material, a second layer of conductive material, a storage capacitor pixel electrode, an insulator and a storage capacitor gate electrode. The application discloses several embodiments, especially one of the embodiments as illustrated in figure 2A, which shows a storage capacitor comprising a pixel electrode (14), an insulator (30) and a gate electrode (10), and another embodiment, as illustrated in figures 4A and 4B and as described "Capacitor 92' is shown in this exemplary embodiment also with dielectric layer 54', semiconductor layer 56', semiconductor contact 58' and an electrode layer", page 10, lines 21-23, which is not clear the capacitor 92' comprising layers 54', 56', 58' and electrode layer. Accordingly, the application does not describe the claimed limitations in such a way as to enable examiner to understand the claimed invention, i.e., which figure corresponding to the claimed invention as recited in claim above, which reference numbers corresponding to the claimed insulating material layer of the claimed storage capacitor, the claimed first conductive material layer of the claimed storage capacitor, the claimed conductive material second layer of the claimed storage capacitor and the claimed storage capacitor pixel electrode, the claimed insulator and the claimed storage capacitor gate electrode, as recited in the claim above.

As per claims 10-12, since these claims depend on claim 9, these claims are also rejected for the same reason as set forth in claim 9 above.

As per claim 13, when this claim is read together with independent claim 1, this claim recites a storage capacitor comprising a layer of insulating material, a first layer of conductive material, a second layer of conductive material, a storage capacitor pixel electrode, a semiconductor, an insulator and a storage capacitor gate electrode. The application discloses several embodiments, especially one of the embodiments as illustrated in figure 2B, which shows a storage capacitor comprising a pixel electrode (14), a semiconductor layer (40), an insulator (30) and a gate electrode (10), and another embodiment, as illustrated in figures 4A and 4B and as described "Capacitor 92' is shown in this exemplary embodiment also with dielectric layer 54', semiconductor layer 56', semiconductor contact 58' and an electrode layer", page 10, lines 21-23, which is not clear the capacitor 92' comprising layers 54', 56', 58' and electrode layer. Accordingly, the application does not describe the claimed limitations in such a way as to enable examiner to understand the claimed invention, i.e., which figure corresponding to the claimed invention as recited in claim above, which reference numbers corresponding to the claimed insulating material layer of the claimed storage capacitor, the claimed first conductive material layer of the claimed storage capacitor, the claimed conductive material second layer of the claimed storage capacitor and the claimed storage capacitor pixel electrode, the claimed semiconductor layer, the claimed insulator and the claimed storage capacitor gate electrode, as recited in the claim above.

As per claim 14, when this claim is read together with independent claim 1, this claim recites a storage capacitor comprising a layer of insulating material, a first layer of conductive

material, a second layer of conductive material, a storage capacitor pixel electrode, an insulator and a conductor. The application discloses several embodiments, especially one of the embodiments as illustrated in figure 2D, which shows a storage capacitor comprising a pixel electrode (14), an insulator (30) and a conductor (16), and another embodiment, as illustrated in figures 4A and 4B and as described "Capacitor 92' is shown in this exemplary embodiment also with dielectric layer 54', semiconductor layer 56', semiconductor contact 58' and an electrode layer", page 10, lines 21-23, which is not clear the capacitor 92' comprising layers 54', 56', 58' and electrode layer. Accordingly, the application does not describe the claimed limitations in such a way as to enable examiner to understand the claimed invention, i.e., which figure corresponding to the claimed invention as recited in claim above, which reference numbers corresponding to the claimed insulating material layer of the claimed storage capacitor, the claimed first conductive material layer of the claimed storage capacitor, the claimed conductive material second layer of the claimed storage capacitor and the claimed storage capacitor pixel electrode, the claimed insulator and the claimed conductor, as recited in the claim above.

As per claims 19 and 20, the application does not describe the claimed limitations in such a way as to enable examiner to understand the claimed invention as recited in these claims, e.g., there is no figure to illustrate the method of addressing an electronic display along with the detailed description (also see the drawing objection above). These claims are therefore rejected for the reason as set forth above.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1, 3-17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morin et al. (USPN: 5,238,861, cited in IDS filed on 02/05/01).

As per claims 1, 3-6, 9-13, 16, 17, 19 and 20, Morin et al. disclose an active matrix liquid crystal display device (corresponding to the claimed electronic display) and an associate method of addressing the electronic display device (col. 1, lines 27-68), the display comprising a liquid crystal display medium (corresponding to the claimed encapsulated display medium) encapsulated between two plates and comprising a plurality of pixels (col. 1, lines 13-19); a TFT transistor (see fig. 2a) having a drain electrode connected to a column line (Cn) (corresponding to the claimed data electrode), a gate electrode connected to an addressing line (Ln) (corresponding to the claimed gate electrode), a source electrode connected to a storage capacitor (Cs) (corresponding to the claimed pixel electrode), a layer (corresponding to the claimed layer of insulating material) including a semiconductive film (14) (corresponding to the claimed layer of semiconductive material) and a non-conductive film (16) (corresponding to the claimed insulator layer), a metallic film (18) (corresponding to the claimed first layer of conductive material) and a film of transparent conductive material (12) (corresponding to the claimed second layer of conductive material) (see fig. 4a and 12); and a storage capacitor (Cs) (corresponding to the claimed storage capacitor) comprising a layer (corresponding to the claimed layer of insulating material) including a semiconductive film (14) (corresponding to the claimed layer of semiconductive material) and a non-conductive film (16) (corresponding to the claimed insulator layer), a metallic film (18) (corresponding to the claimed first layer of

conductive material) and a film of transparent conductive material (12) (corresponding to the claimed second layer of conductive material) (see fig. 4b and 12). As noting in figure 1a, one skill in the art would recognize that in the case of no storage capacitor present, Morin et al. disclose the pixel representing as a parallel capacitor Clc (corresponding to the claimed capacitance of the pixel) tied to a counter electrode (Vce) and an inherent resistor (R) (corresponding to the claimed resistance of the pixel), so that the voltage decay time across the pixel is based on the product of R and Clc. Further, as noting in figure 1b, one skill in the art would recognize that in the case of storage capacitor (Cs) present, Morin et al. obviously disclose the voltage decay time across the pixel is based on the product of R and (Clc + Cs) (since Clc and Cs are parallel in connection). Accordingly, adding the storage capacitor increases the voltage decay time and thereby reduces a rate of voltage decay across the pixel. Therefore, these claims are rejected for the reason as set forth above.

In regard to claim 7 as applied to claim1 above, as noting in figure 2b, Morin et al. further teach the storage capacitor in electrical communication with a second gate line (Ln) different from a first gate line (Ln+1) in electrical communication with the transistor gate electrode for addressing the pixel. Therefore, this claim is rejected for the reason as set forth above.

In regard to claim 8 as applied to claim1 above, as noting in figure 2a, Morin et al. further teach the storage capacitor in electrical communication with a capacitive electrode (Lc) (corresponding to the claimed conductor). Therefore, this claim is rejected for the reason as set forth above.

In regard to claim 14 as applied to claim1 above, as noting in figure 4b, Morin et al. further teach the storage capacitor comprising block (P) (corresponding to the claimed storage capacitor pixel electrode, an insulator including a semiconductive film (14) and a non-conductive (16), and a capacitive line (Lc) (corresponding to the claimed conductor). Therefore, this claim is rejected for the reason as set forth above.

In regard to claim 15 as applied to claim1 above, as noting at col. 5, lines 32-40, Morin et al. further teach that the capacitance of storage capacitor is about 1pf and the capacitance of the pixel is about 0.5pf. Accordingly, Mori et al. obviously disclose the claimed invention as specified in claim, and this claim is therefore rejected for the reason as set forth above.

12. Claims 2 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morin et al. in view of Spitzer et al. (USPN: 6,140,980).

Regarding to claim 2 as applied to claim 1 above, as described above, Morin et al. disclose the display comprising a liquid crystal display medium encapsulated between two plates and comprising a plurality of pixels (col. 1, lines 13-19), but does not disclose expressly an electrophoretic display medium, as claimed. Accordingly, Morin et al. disclose the claimed subject matter except for a LCD medium instead of an electrophoretic display medium.

However, Spitzer et al. disclose a related electronic display comprising a storage capacitor (56) (fig. 3, col. 6, lines 10-16). As noting at col. 30, lines 40-49, Spitzer et al. further teach that the invention can be implemented in LCD, electrophoretic display or other type displays.

It would have been obvious to a person of ordinary skill in the art to utilize Spitzer et al.'s teaching in the electronic display of Morin et al. because this would obviously provide an

electrophoretic display adaptable in some particular applications and having the same benefits as well as the LCD device. Therefore, it would have been obvious to combine Spitzer et al with Morin et al. to obtain the invention as specified in claim above.

As per claim 18, since this claim recites all limitations read in claim 2 above, this claim is therefore rejected for the same reason as set forth in claim 2 above.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is (703) 306-5422. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at (703) 305-4938.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

JHN
May 30, 2002

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600